WHAT IS CLAIMED IS:

1. A data recovery method for generating a recovered clock signal from input data and taking in said input data on the basis of a timing of said recovered clock signal,

wherein a position of an edge of said input data is compared with a position of an edge of said recovered clock signal, and said edge of said recovered clock signal is kept away from said edge of said input data if a gap between said edge of said recovered clock signal and said edge of said input data becomes smaller than a reference value.

2. A data recovery method according to claim 1, wherein a cycle of a reference clock signal is divided into N portions to generate N clock signals with phases different from each other, and one of said N clock signals is selected as said recovered clock signal.

3. A digital-control type clock data recovery circuit comprising:

a phase comparator for comparing a phase of input data with a phase of a data recovery clock signal generated internally and outputting shift directions of said phase of said data recovery clock signal as UP and DOWN signals;

a counter for controlling a frequency at which said UP and DOWN signals are fed back to a means for determining said phase of said data recovery clock signal;

a cyclic clock-phase pointer for generating a phase

control signal for controlling said determined phase of said data recovery clock signal on the basis of OUT UP and OUT DOWN signals output by said counter; and

a phase variable-delay circuit for outputting a clock signal according to said phase control signal as said data recovery clock signal;

wherein said input data is taken in with a timing of said data recovery clock signal.

4. A digital-control type clock data recovery circuit according to claim 3, wherein said phase variable-delay circuit changes said phase of said data recovery clock signal so as to separate said edge of said recovered clock signal away from said edge of said input data by a predetermined time gap.

5. A digital-control type clock data recovery circuit according to claim 3, wherein said phase variable-delay circuit divides a reference clock signal into N portions to generate N clock signals with phases different from each other, and selects one of said N clock signals as said recovered clock signal in accordance with said phase control signal.

6. A digital-control type clock data recovery circuit according to claim 3, wherein said phase variable-delay circuit selects one phase to be output by said phase variable-delay circuit on the basis of a plurality of results of phase detection carried out over a plurality of cycles having a phase-switching pitch Tp equal to or smaller than a value determined by said cyclic clock-phase pointer.

7. A digital-control type clock data recovery circuit according to claim 3, wherein said phase variable-delay circuit comprising a buffer, a composition circuit, an N-1 selector and a CMOS level conversion circuit, and said buffer, said composition circuit, said N-1 selector and said CMOS level conversion circuit are each designed as a small-amplitude differential circuit.

8. A digital-control type clock data recovery circuit according to claim 7, wherein, by executing control to turn on 2 of said N selector control signals supplied to each 2 adjacent pins of said N-1 selector at the same time, said N-1 selector is capable of generating a middle phase between first and second phases and, hence, obtaining N × 2 phases from N input phases.

9. A digital-control type clock data recovery circuit having a function to track a wander of input data by comparing a position of an edge of said input data with a position of an edge of a clock signal.

10. A digital-control type clock data recovery circuit according to claim 9, wherein said function to track a wander of input data by comparing a position of an edge of said input data with a position of an edge of a clock signal is executed under a condition expressed by a relation given as follows:

$$B \times \sin(2p \times Ta/Tw) < T/N$$

where symbol B denotes a maximum phase change of said input data over a long period of time, symbol Ta denotes a loop delay, which is a period of time between an output operation carried out by

a counter and a first phase comparison, symbol Tw denotes a phase deviation period, symbol T denotes a clock period, symbol N denotes the number of phase divisions, and T/N denotes a difference between 2 adjacent phases determined by said number of phase divisions N.

11. A digital-control type clock data recovery circuit having a control circuit for comparing a position of an edge of data with a position of an edge of a data recovery clock signal to execute control for placing said edge of said data recovery clock signal in an eye narrowed by high-frequency phase deviations (jitters) of said data, wherein said data is taken in with a timing of said edge of said data recovery clock signal.

12. A digital-control type clock data recovery circuit according to claim 11, wherein said control circuit executes said control for placing said edge of said data recovery clock signal in an eye narrowed by high-frequency phase deviations (jitters) of said data by execution of control to prevent a distance between said position of said edge of said data recovery clock signal and said position of said edge of said data from becoming smaller than a predetermined value.

13. A digital-control type clock data recovery circuit according to claim 11, wherein said control circuit compares said position of said edge of said data recovery clock signal with said position of said edge of said data at a first predetermined frequency and changes a phase of said data recovery clock signal at a second predetermined frequency not

exceeding said first predetermined frequency.